Abstract of the Disclosure:

A circuit configuration for the bit-parallel outputting the bits of a data word includes at least two signal lines for feeding the data signals representing the bits of the data word to driver stages and to a reference circuit. Further driver stages are connected in parallel with the driver stages and have inputs connected to the control device. The control device establishes the signal states of the data signals to be transferred on each signal line and generates a control signal depending on the type and number of the signal state changes of bit sequences to be transferred. It is possible to drive the driver stages that assigned to the signal line for which a signal state change is present.

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